

	L #	Hits	Search Text	DBs
1	L1	14876	(instruction prefetch\$3 fetch\$3) near5 (queue buffer)	USPAT; US-PGPUB
2	L2	2862	1 near20 cache	USPAT; US-PGPUB
3	L3	1601	1 near50 branch	USPAT; US-PGPUB
4	L4	2224	1 near20 (select\$3 multiplex\$3)	USPAT; US-PGPUB
5	L7	154	3 near99 4	USPAT; US-PGPUB
6	L8	813	1 near20 target	USPAT; US-PGPUB
7	L12	303	3 near99 8 and 2	USPAT; US-PGPUB
8	L13	242	12 not 7	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040 03086 6 A1	<input type="checkbox"/>	Apparatus and method for buffering instructions and late-generated related information using history of previous loadshifts	712/217
2	US 20040 01568 3 A1	<input checked="" type="checkbox"/>	Two dimensional branch history table prefetching mechanism	712/240
3	US 20040 00329 8 A1	<input checked="" type="checkbox"/>	Icache and general array power reduction method for loops	713/300
4	US 20040 00320 3 A1	<input checked="" type="checkbox"/>	Instruction fetch control device and instruction fetch control method	712/205
5	US 20030 22600 3 A1	<input checked="" type="checkbox"/>	Information processor having delayed branch function	712/238
6	US 20030 22599 8 A1	<input checked="" type="checkbox"/>	Configurable data processor with multi-length instruction set architecture	712/210
7	US 20030 14020 3 A1	<input checked="" type="checkbox"/>	Memory record update filtering	711/159
8	US 20030 13121 2 A1	<input checked="" type="checkbox"/>	Absolute address bits kept in branch history table	711/203
9	US 20030 07006 2 A1	<input checked="" type="checkbox"/>	System and method for reducing computing system latencies associated with branch instructions	712/234
10	US 20030 02875 8 A1	<input checked="" type="checkbox"/>	SINGLE ARRAY BANKED BRANCH TARGET BUFFER	712/238
11	US 20020 19909 2 A1	<input checked="" type="checkbox"/>	Split history tables for branch prediction	712/240
12	US 20020 19446 1 A1	<input checked="" type="checkbox"/>	Speculative branch target address cache	712/238
13	US 20020 14379 9 A1	<input checked="" type="checkbox"/>	Memory record update filtering	707/200
14	US 20020 10802 9 A1	<input checked="" type="checkbox"/>	Program counter (PC) relative addressing mode with fast displacement	712/234
15	US 20020 09556 6 A1	<input checked="" type="checkbox"/>	METHOD FOR PROCESSING BRANCH OPERATIONS	712/239
16	US 20010 05414 0 A1	<input checked="" type="checkbox"/>	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
17	US 20010 05205 3 A1	<input checked="" type="checkbox"/>	Stream processing unit for a multi-streaming processor	711/138

	Document ID	U	Title	Current OR
18	US 20010 05196 9 A1	<input checked="" type="checkbox"/>	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/514
19	US 20010 03230 9 A1	<input checked="" type="checkbox"/>	Static branch prediction mechanism for conditional branch instructions	712/239
20	US 20010 02751 5 A1	<input checked="" type="checkbox"/>	Apparatus and method of controlling instruction fetch	712/207
21	US 20010 02342 5 A1	<input checked="" type="checkbox"/>	Method and apparatus for rounding in a multiplier arithmetic	708/620
22	US 20010 01005 1 A1	<input checked="" type="checkbox"/>	Method and apparatus for multi-function arithmetic	708/502
23	US 66979 37 B1	<input checked="" type="checkbox"/>	Split history tables for branch prediction	712/240
24	US 66788 08 B2	<input checked="" type="checkbox"/>	Memory record update filtering	711/159
25	US 66622 97 B1	<input checked="" type="checkbox"/>	Allocation of processor bandwidth by inserting interrupt servicing instructions to intervene main program in instruction queue mechanism	712/245
26	US 66119 10 B2	<input checked="" type="checkbox"/>	Method for processing branch operations	712/237
27	US 66041 91 B1	<input checked="" type="checkbox"/>	Method and apparatus for accelerating instruction fetching for a processor	712/207
28	US 65713 31 B2	<input checked="" type="checkbox"/>	Static branch prediction mechanism for conditional branch instructions	712/239
29	US 65570 98 B2	<input checked="" type="checkbox"/>	Microprocessor including an efficient implementation of extreme value instructions	712/223
30	US 65534 69 B2	<input checked="" type="checkbox"/>	Memory record update filtering	711/159
31	US 65464 81 B1	<input checked="" type="checkbox"/>	Split history tables for branch prediction	712/240
32	US 65325 21 B1	<input checked="" type="checkbox"/>	Mechanism for high performance transfer of speculative request data between levels of cache hierarchy	711/137
33	US 65131 09 B1	<input checked="" type="checkbox"/>	Method and apparatus for implementing execution predicates in a computer processing system	712/200
34	US 65104 94 B1	<input checked="" type="checkbox"/>	Time based mechanism for cached speculative data deallocation	711/137
35	US 64991 23 B1	<input checked="" type="checkbox"/>	Method and apparatus for debugging an integrated circuit	714/724
36	US 64991 01 B1	<input checked="" type="checkbox"/>	Static branch prediction mechanism for conditional branch instructions	712/239
37	US 64969 21 B1	<input checked="" type="checkbox"/>	Layered speculative request unit with instruction optimized and storage hierarchy optimized partitions	712/207
38	US 64876 37 B1	<input checked="" type="checkbox"/>	Method and system for clearing dependent speculations from a request queue	711/133

	Document ID	U	Title	Current OR
39	US 64776 39 B1	<input checked="" type="checkbox"/>	Branch instruction mechanism for processor	712/237
40	US 64738 33 B1	<input checked="" type="checkbox"/>	Integrated cache and directory structure for multi-level caches	711/122
41	US 64534 12 B1	<input checked="" type="checkbox"/>	Method and apparatus for reissuing paired MMX instructions singly during exception handling	712/244
42	US 64461 97 B1	<input checked="" type="checkbox"/>	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
43	US 64426 81 B1	<input checked="" type="checkbox"/>	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
44	US 64386 56 B1	<input checked="" type="checkbox"/>	Method and system for cancelling speculative cache prefetch requests	711/137
45	US 64272 04 B1	<input checked="" type="checkbox"/>	Method for just in-time delivery of instructions in a data processing system	712/206
46	US 64271 92 B1	<input checked="" type="checkbox"/>	Method and apparatus for caching victimized branch predictions	711/133
47	US 64250 75 B1	<input checked="" type="checkbox"/>	Branch prediction device with two levels of branch prediction cache	712/239
48	US 64217 63 B1	<input checked="" type="checkbox"/>	Method for instruction extensions for a tightly coupled speculative request unit	711/137
49	US 64217 62 B1	<input checked="" type="checkbox"/>	Cache allocation policy based on speculative request history	711/130
50	US 64216 96 B1	<input checked="" type="checkbox"/>	System and method for high speed execution of Fast Fourier Transforms utilizing SIMD instructions on a general purpose processor	708/404
51	US 64185 16 B1	<input checked="" type="checkbox"/>	Method and system for managing speculative requests in a multi-level memory hierarchy	711/138
52	US 64120 50 B1	<input checked="" type="checkbox"/>	Memory record update filtering	711/159
53	US 64011 93 B1	<input checked="" type="checkbox"/>	Dynamic data prefetching based on program counter and addressing mode	712/207
54	US 63972 39 B2	<input checked="" type="checkbox"/>	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/505
55	US 63972 38 B2	<input checked="" type="checkbox"/>	Method and apparatus for rounding in a multiplier	708/497
56	US 63935 54 B1	<input checked="" type="checkbox"/>	Method and apparatus for performing vector and scalar multiplication and calculating rounded products	712/221
57	US 63935 28 B1	<input checked="" type="checkbox"/>	Optimized cache allocation algorithm for multiple speculative requests	711/137
58	US 63935 23 B1	<input checked="" type="checkbox"/>	Mechanism for invalidating instruction cache blocks in a pipeline processor	711/125
59	US 63816 25 B2	<input checked="" type="checkbox"/>	Method and apparatus for calculating a power of an operand	708/606
60	US 63743 50 B1	<input checked="" type="checkbox"/>	System and method of maintaining and utilizing multiple return stack buffers	712/239

	Document ID	U	Title	Current OR
61	US 63743 48 B1	<input checked="" type="checkbox"/>	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
62	US 63602 99 B1	<input checked="" type="checkbox"/>	Extended cache state with prefetched stream ID information	711/137
63	US 63569 97 B1	<input checked="" type="checkbox"/>	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
64	US 63518 01 B1	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
65	US 63246 43 B1	<input checked="" type="checkbox"/>	Branch prediction and target instruction control for processor	712/237
66	US 63112 61 B1	<input checked="" type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
67	US 62983 67 B1	<input checked="" type="checkbox"/>	Floating point addition pipeline including extreme value, comparison and accumulate functions	708/524
68	US 62693 84 B1	<input checked="" type="checkbox"/>	Method and apparatus for rounding and normalizing results within a multiplier	708/497
69	US 62634 27 B1	<input checked="" type="checkbox"/>	Branch prediction mechanism	712/236
70	US 62567 28 B1	<input checked="" type="checkbox"/>	Processor configured to selectively cancel instructions from its pipeline responsive to a predicted-taken short forward branch instruction	712/236
71	US 62566 53 B1	<input checked="" type="checkbox"/>	Multi-function bipartite look-up table	708/290
72	US 62508 21 B1	<input checked="" type="checkbox"/>	Method and apparatus for processing branch instructions in an instruction buffer	712/238
73	US 62471 24 B1	<input checked="" type="checkbox"/>	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
74	US 62471 20 B1	<input checked="" type="checkbox"/>	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
75	US 62370 83 B1	<input checked="" type="checkbox"/>	Microprocessor including multiple register files mapped to the same logical storage and inhibiting synchronization between the register files responsive to inclusion of an instruction in an instruction sequence	712/217
76	US 62336 76 B1	<input checked="" type="checkbox"/>	Apparatus and method for fast forward branch	712/233
77	US 62231 98 B1	<input checked="" type="checkbox"/>	Method and apparatus for multi-function arithmetic	708/620
78	US 62231 92 B1	<input checked="" type="checkbox"/>	Bipartite look-up table with output values having minimized absolute error	708/270
79	US 62162 19 B1	<input checked="" type="checkbox"/>	Microprocessor circuits, systems, and methods implementing a load target buffer with entries relating to prefetch desirability	712/207
80	US 62126 29 B1	<input checked="" type="checkbox"/>	Method and apparatus for executing string instructions	712/241
81	US 61991 52 B1	<input checked="" type="checkbox"/>	Translated memory protection apparatus for an advanced microprocessor	711/207
82	US 61957 35 B1	<input checked="" type="checkbox"/>	Prefetch circuitry for prefetching variable size data	711/204

	Document ID	U	Title	Current OR
83	US 61758 97 B1	<input checked="" type="checkbox"/>	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
84	US 61700 54 B1	<input checked="" type="checkbox"/>	Method and apparatus for predicting target addresses for return from subroutine instructions utilizing a return address cache	712/242
85	US 61516 71 A	<input checked="" type="checkbox"/>	System and method of maintaining and utilizing multiple return stack buffers	712/239
86	US 61449 80 A	<input checked="" type="checkbox"/>	Method and apparatus for performing multiple types of multiplication including signed and unsigned multiplication	708/627
87	US 61345 74 A	<input checked="" type="checkbox"/>	Method and apparatus for achieving higher frequencies of exactly rounded results	708/551
88	US 61311 04 A	<input checked="" type="checkbox"/>	Floating point addition pipeline configured to perform floating point-to-integer and integer-to-floating point conversion operations	708/204
89	US 61157 33 A	<input checked="" type="checkbox"/>	Method and apparatus for calculating reciprocals and reciprocal square roots	708/654
90	US 61157 32 A	<input checked="" type="checkbox"/>	Method and apparatus for compressing intermediate products	708/625
91	US 61120 19 A	<input checked="" type="checkbox"/>	Distributed instruction queue	712/214
92	US 60946 68 A	<input checked="" type="checkbox"/>	Floating point arithmetic unit including an efficient close data path	708/505
93	US 60887 93 A	<input checked="" type="checkbox"/>	Method and apparatus for branch execution on a multiple-instruction-set-architecture microprocessor	712/239
94	US 60887 15 A	<input checked="" type="checkbox"/>	Close path selection unit for performing effective subtraction within a floating point arithmetic unit	708/505
95	US 60852 13 A	<input checked="" type="checkbox"/>	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and summing the products	708/603
96	US 60852 12 A	<input checked="" type="checkbox"/>	Efficient method for performing close path subtraction in a floating point arithmetic unit	708/505
97	US 60852 08 A	<input checked="" type="checkbox"/>	Leading one prediction unit for normalizing close path subtraction results within a floating point arithmetic unit	708/205
98	US 60676 16 A	<input checked="" type="checkbox"/>	Branch prediction device with two levels of branch prediction cache	712/239
99	US 60651 10 A	<input checked="" type="checkbox"/>	Method and apparatus for loading an instruction buffer of a processor capable of out-of-order instruction issue	712/217
100	US 60584 65 A	<input checked="" type="checkbox"/>	Single-instruction-multiple-data processing in a multimedia signal processor	712/7
101	US 60527 08 A	<input checked="" type="checkbox"/>	Performance monitoring of thread switch events in a multithreaded processor	718/108
102	US 60444 59 A	<input checked="" type="checkbox"/>	Branch prediction apparatus having branch target buffer for effectively processing branch instruction	712/237
103	US 60385 83 A	<input checked="" type="checkbox"/>	Method and apparatus for simultaneously multiplying two or more independent pairs of operands and calculating a rounded products	708/628
104	US 60353 86 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
105	US 60319 92 A	<input checked="" type="checkbox"/>	Combining hardware and software to provide an improved microprocessor	717/138

	Document ID	U	Title	Current OR
106	US 60292 44 A	<input checked="" type="checkbox"/>	Microprocessor including an efficient implementation of extreme value instructions	712/223
107	US 60292 28 A	<input checked="" type="checkbox"/>	Data prefetching of a load target buffer for post-branch instructions based on past prediction accuracy's of branch predictions	711/137
108	US 60264 83 A	<input checked="" type="checkbox"/>	Method and apparatus for simultaneously performing arithmetic on two or more pairs of operands	712/221
109	US 60121 25 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including a decoded instruction cache configured to receive partially decoded instructions	711/125
110	US 60119 08 A	<input checked="" type="checkbox"/>	Gated store buffer for an advanced microprocessor	714/19
111	US 59960 71 A	<input checked="" type="checkbox"/>	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
112	US 59788 96 A	<input checked="" type="checkbox"/>	Method and system for increased instruction dispatch efficiency in a superscalar processor system	712/23
113	US 59742 60 A	<input checked="" type="checkbox"/>	Data processor to control a sequence of instructions to be executed by rearranging the instruction blocks	712/32
114	US 59648 68 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a speculative return stack buffer	712/234
115	US 59580 61 A	<input checked="" type="checkbox"/>	Host microprocessor with apparatus for temporarily holding target processor state	714/1
116	US 59548 15 A	<input checked="" type="checkbox"/>	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
117	US 59535 12 A	<input checked="" type="checkbox"/>	Microprocessor circuits, systems, and methods implementing a loop and/or stride predicting load target buffer	712/205
118	US 59516 79 A	<input checked="" type="checkbox"/>	Microprocessor circuits, systems, and methods for issuing successive iterations of a short backward branch loop in a single cycle	712/241
119	US 59467 05 A	<input checked="" type="checkbox"/>	Avoidance of cache synonyms	711/108
120	US 59448 18 A	<input checked="" type="checkbox"/>	Method and apparatus for accelerated instruction restart in a microprocessor	712/244
121	US 59419 83 A	<input checked="" type="checkbox"/>	Out-of-order execution using encoded dependencies between instructions in queues to determine stall values that control issuance of instructions from the queues	712/214
122	US 59419 80 A	<input checked="" type="checkbox"/>	Apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system	712/204
123	US 59319 44 A	<input checked="" type="checkbox"/>	Branch instruction handling in a self-timed marking system	712/239
124	US 59268 32 A	<input checked="" type="checkbox"/>	Method and apparatus for aliasing memory data in an advanced microprocessor	711/141
125	US 59260 53 A	<input checked="" type="checkbox"/>	Selectable clock generation mode	327/298
126	US 59180 62 A	<input checked="" type="checkbox"/>	Microprocessor including an efficient implementation of an accumulate instruction	712/7
127	US 59180 46 A	<input checked="" type="checkbox"/>	Method and apparatus for a branch instruction pointer table	712/239

	Document ID	U	Title	Current OR
128	US 59095 66 A	<input checked="" type="checkbox"/>	Microprocessor circuits, systems, and methods for speculatively executing an instruction using its most recently used data while concurrently prefetching data for the instruction	712/207
129	US 58988 66 A	<input checked="" type="checkbox"/>	Method and apparatus for counting remaining loop instructions and pipelining the next instruction	712/241
130	US 58964 93 A	<input checked="" type="checkbox"/>	Raid algorithm using a multimedia functional unit	714/6
131	US 58922 49 A	<input checked="" type="checkbox"/>	Integrated circuit having reprogramming cell	257/209
132	US 58706 12 A	<input checked="" type="checkbox"/>	Method and apparatus for condensed history buffer	710/260
133	US 58676 83 A	<input checked="" type="checkbox"/>	Method of operating a high performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
134	US 58676 82 A	<input checked="" type="checkbox"/>	High performance superscalar microprocessor including a circuit for converting CISC instructions to RISC operations	712/210
135	US 58647 07 A	<input checked="" type="checkbox"/>	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
136	US 58600 96 A	<input checked="" type="checkbox"/>	Multi-level instruction cache for a computer	711/122
137	US 58600 14 A	<input checked="" type="checkbox"/>	Method and apparatus for improved recovery of processor state using history buffer	710/260
138	US 58570 89 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
139	US 58505 43 A	<input checked="" type="checkbox"/>	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238
140	US 58482 68 A	<input checked="" type="checkbox"/>	Data processor with branch target address generating unit	712/233
141	US 58420 08 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a branch target buffer cache with multiple BTB banks	712/240
142	US 58389 84 A	<input checked="" type="checkbox"/>	Single-instruction-multiple-data processing using multiple banks of vector registers	712/5
143	US 58389 44 A	<input checked="" type="checkbox"/>	System for storing processor register data after a mispredicted branch	712/218
144	US 58359 67 A	<input checked="" type="checkbox"/>	Adjusting prefetch size based on source of prefetch address	711/213
145	US 58359 S1 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
146	US 58322 59 A	<input checked="" type="checkbox"/>	Apparatus for superscalar instruction pre-decoding using cached instruction lengths	712/238
147	US 58322 05 A	<input checked="" type="checkbox"/>	Memory controller for a microprocessor for detecting a failure of speculation on the physical nature of a component being addressed	714/53
148	US 58225 76 A	<input checked="" type="checkbox"/>	Branch history table with branch pattern field	712/239
149	US 58190 56 A	<input checked="" type="checkbox"/>	Instruction buffer organization method and system	712/204

	Document ID	U	Title	Current OR
150	US 58156 93 A	<input checked="" type="checkbox"/>	Processor having a frequency modulated core clock based on the criticality of program activity	713/501
151	US 58156 92 A	<input checked="" type="checkbox"/>	Distributed clock generator	713/501
152	US 58128 39 A	<input checked="" type="checkbox"/>	Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit	712/239
153	US 58058 78 A	<input checked="" type="checkbox"/>	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239
154	US 58058 53 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
155	US 57991 62 A	<input checked="" type="checkbox"/>	Program counter update mechanism	712/205
156	US 57817 83 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamically adjusting the power consumption of a circuit block within an integrated circuit	713/320
157	US 57817 53 A	<input checked="" type="checkbox"/>	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
158	US 57784 35 A	<input checked="" type="checkbox"/>	History-based prefetch cache including a time queue	711/137
159	US 57782 46 A	<input checked="" type="checkbox"/>	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
160	US 57747 10 A	<input checked="" type="checkbox"/>	Cache line branch prediction scheme that shares among sets of a set associative cache	712/238
161	US 57685 76 A	<input checked="" type="checkbox"/>	Method and apparatus for predicting and handling resolving return from subroutine instructions in a computer processor	712/238
162	US 57685 75 A	<input checked="" type="checkbox"/>	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/228
163	US 57652 20 A	<input checked="" type="checkbox"/>	Apparatus and method to reduce instruction address storage in a super-scaler processor	711/220
164	US 57649 70 A	<input checked="" type="checkbox"/>	Method and apparatus for supporting speculative branch and link/branch on count instructions	712/233
165	US 57649 38 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/200
166	US 57614 90 A	<input checked="" type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
167	US 57581 20 A	<input checked="" type="checkbox"/>	Method and system for increased system memory concurrency in a multi-processor computer system utilizing concurrent access of reference and change bits	711/150
168	US 57519 81 A	<input checked="" type="checkbox"/>	High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format	712/204
169	US 57489 32 A	<input checked="" type="checkbox"/>	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
170	US 57404 19 A	<input checked="" type="checkbox"/>	Processor and method for speculatively executing an instruction loop	712/241

	Document ID	U	Title	Current OR
171	US 57404 17 A	<input checked="" type="checkbox"/>	Pipelined processor operating in different power mode based on branch prediction state of branch history bit encoded as taken weakly not taken and strongly not taken states	712/239
172	US 57404 16 A	<input checked="" type="checkbox"/>	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
173	US 57404 15 A	<input checked="" type="checkbox"/>	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238
174	US 57404 10 A	<input checked="" type="checkbox"/>	Static clock generator	713/501
175	US 57403 92 A	<input checked="" type="checkbox"/>	Method and apparatus for fast decoding of 00H and OFH mapped instructions	712/210
176	US 57403 91 A	<input checked="" type="checkbox"/>	Preventing premature early exception signaling with special instruction encoding	712/200
177	US 57377 50 A	<input checked="" type="checkbox"/>	Partitioned single array cache memory having first and second storage regions for storing non-branch and branch instructions	711/129
178	US 57375 90 A	<input checked="" type="checkbox"/>	Branch prediction system using limited branch target buffer updates	712/238
179	US 57348 81 A	<input checked="" type="checkbox"/>	Detecting short branches in a prefetch buffer using target location information in a branch target cache	712/238
180	US 57322 53 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
181	US 57322 43 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
182	US 57271 77 A	<input checked="" type="checkbox"/>	Reorder buffer circuit accommodating special instructions operating on odd-width results	712/218
183	US 57218 55 A	<input checked="" type="checkbox"/>	Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer	712/218
184	US 57218 54 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic conversion of computer instructions	712/203
185	US 57178 92 A	<input checked="" type="checkbox"/>	Selectively operable cache memory	711/128
186	US 57064 91 A	<input checked="" type="checkbox"/>	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
187	US 57014 48 A	<input checked="" type="checkbox"/>	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
188	US 56969 55 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
189	US 56921 68 A	<input checked="" type="checkbox"/>	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
190	US 56921 67 A	<input checked="" type="checkbox"/>	Method for verifying the correct processing of pipelined instructions including branch instructions and self-modifying code in a microprocessor	712/226
191	US 56873 49 A	<input checked="" type="checkbox"/>	Data processor with branch target address cache and subroutine return address cache and method of operation	711/137
192	US 56641 36 A	<input checked="" type="checkbox"/>	High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations	712/208
193	US 56550 98 A	<input checked="" type="checkbox"/>	High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format	712/210

	Document ID	U	Title	Current OR
194	US 56550 97 A	<input checked="" type="checkbox"/>	High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format	712/204
195	US 56511 25 A	<input checked="" type="checkbox"/>	High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations	712/218
196	US 56492 25 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/23
197	US 56491 45 A	<input checked="" type="checkbox"/>	Data processor processing a jump instruction	711/213
198	US 56491 37 A	<input checked="" type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
199	US 56341 03 A	<input checked="" type="checkbox"/>	Method and system for minimizing branch misprediction penalties within a processor	712/235
200	US 56320 23 A	<input type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218

	Document ID	U	Title	Current OR
1	US 20040 00321 6 A1	<input type="checkbox"/>	Branch prediction apparatus and method	712/237
2	US 20040 00320 2 A1	<input checked="" type="checkbox"/>	Instruction fetch control apparatus	712/205
3	US 20030 20470 5 A1	<input checked="" type="checkbox"/>	Prediction of branch instructions in a data processing apparatus	712/207
4	US 20030 09754 9 A1	<input checked="" type="checkbox"/>	Predicted return address selection upon matching target in branch history table with entries in return address stack	712/240
5	US 20030 00526 2 A1	<input checked="" type="checkbox"/>	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
6	US 20030 00468 3 A1	<input checked="" type="checkbox"/>	Instruction pre-fetching mechanism for a multithreaded program execution	702/186
7	US 20020 19909 1 A1	<input checked="" type="checkbox"/>	Apparatus for branch prediction based on history table	712/240
8	US 20020 18880 8 A1	<input checked="" type="checkbox"/>	Random generator	711/133
9	US 20020 14408 7 A1	<input checked="" type="checkbox"/>	Architecture of method for fetching microprocessor's instructions	712/207
10	US 20020 12082 9 A1	<input checked="" type="checkbox"/>	Data processer and data processing system	712/207
11	US 20020 09991 0 A1	<input checked="" type="checkbox"/>	High speed low power cacheless computer system	711/117
12	US 20020 09191 6 A1	<input checked="" type="checkbox"/>	Embedded-DRAM-DSP architecture	712/228
13	US 20020 08784 5 A1	<input checked="" type="checkbox"/>	Embedded-DRAM-DSP architecture	712/228
14	US 20020 04042 9 A1	<input checked="" type="checkbox"/>	Embedded-DRAM-DSP architecture	712/228
15	US 20020 01389 4 A1	<input checked="" type="checkbox"/>	Data processor with branch target buffer	712/238
16	US 20010 05413 7 A1	<input checked="" type="checkbox"/>	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11
17	US 20010 04746 7 A1	<input checked="" type="checkbox"/>	METHOD AND APPARATUS FOR BRANCH PREDICTION USING FIRST AND SECOND LEVEL BRANCH PREDICTION TABLES	712/228

	Document ID	U	Title	Current OR
18	US 20010 03744 4 A1	<input checked="" type="checkbox"/>	INSTRUCTION BUFFERING MECHANISM	712/207
19	US 20010 01873 5 A1	<input checked="" type="checkbox"/>	Data processor and data processing system	712/207
20	US 67014 26 B1	<input checked="" type="checkbox"/>	Switching between a plurality of branch prediction processes based on which instruction set is operational wherein branch history data structures are the same for the plurality of instruction sets	712/239
21	US 66878 57 B1	<input checked="" type="checkbox"/>	Microcomputer which can execute a monitor program supplied from a debugging tool	714/38
22	US 66511 62 B1	<input checked="" type="checkbox"/>	Recursively accessing a branch target address cache using a target address previously accessed from the branch target address cache	712/238
23	US 66474 67 B1	<input checked="" type="checkbox"/>	Method and apparatus for high performance branching in pipelined microsystems	711/140
24	US 66314 64 B1	<input checked="" type="checkbox"/>	Instruction pipeline with a branch prefetch when the branch is certain	712/234
25	US 66222 36 B1	<input checked="" type="checkbox"/>	Microprocessor instruction fetch unit for processing instruction groups having multiple branch instructions	712/206
26	US 66091 94 B1	<input checked="" type="checkbox"/>	Apparatus for performing branch target address calculation based on branch type	712/238
27	US 65981 54 B1	<input checked="" type="checkbox"/>	Precoding branch instructions to reduce branch-penalty in pipelined processors	712/237
28	US 65981 53 B1	<input checked="" type="checkbox"/>	Processor and method that accelerate evaluation of pairs of condition-setting and branch instructions	712/234
29	US 65981 52 B1	<input checked="" type="checkbox"/>	Increasing the overall prediction accuracy for multi-cycle branch prediction and apparatus by enabling quick recovery	712/228
30	US 65811 20 B1	<input checked="" type="checkbox"/>	Interrupt controller	710/262
31	US 65534 88 B2	<input checked="" type="checkbox"/>	Method and apparatus for branch prediction using first and second level branch prediction tables	712/239
32	US 65534 80 B1	<input checked="" type="checkbox"/>	System and method for managing the execution of instruction groups having multiple executable instructions	712/23
33	US 65429 82 B2	<input checked="" type="checkbox"/>	Data processor and data processing system	712/207
34	US 65300 16 B1	<input checked="" type="checkbox"/>	Predicted return address selection upon matching target in branch history table with entries in return address stack	712/237
35	US 65231 10 B1	<input checked="" type="checkbox"/>	Decoupled fetch-execute engine with static branch prediction support	712/239
36	US 65052 92 B1	<input checked="" type="checkbox"/>	Processor including efficient fetch mechanism for L0 and L1 caches	712/207
37	US 65021 88 B1	<input checked="" type="checkbox"/>	Dynamic classification of conditional branches in global history branch prediction	712/234
38	US 64776 40 B1	<input checked="" type="checkbox"/>	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
39	US 64704 43 B1	<input checked="" type="checkbox"/>	Pipelined multi-thread processor selecting thread instruction in inter-stage buffer based on count information	712/205

	Document ID	U	Title	Current OR
40	US 64571 17 B1	<input checked="" type="checkbox"/>	Processor configured to predecode relative control transfer instructions and replace displacements therein with a target address	712/213
41	US 64346 91 B1	<input checked="" type="checkbox"/>	Cell phones with instruction pre-fetch buffers allocated to low bit address ranges and having validating flags	712/205
42	US 64185 25 B1	<input checked="" type="checkbox"/>	Method and apparatus for reducing latency in set-associative caches using set prediction	711/213
43	US 63895 31 B1	<input checked="" type="checkbox"/>	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
44	US 63670 06 B1	<input checked="" type="checkbox"/>	Predecode buffer including buffer pointer indicating another buffer for predecoding	712/244
45	US 63670 01 B1	<input checked="" type="checkbox"/>	Processor including efficient fetch mechanism for L0 and L1 caches	712/205
46	US 62928 84 B1	<input checked="" type="checkbox"/>	Reorder buffer employing last in line indication	712/216
47	US 62533 16 B1	<input checked="" type="checkbox"/>	Three state branch history using one bit in a branch prediction mechanism	712/239
48	US 62162 06 B1	<input checked="" type="checkbox"/>	Trace victim cache	711/133
49	US 61991 54 B1	<input checked="" type="checkbox"/>	Selecting cache to fetch in multi-level cache system based on fetch address source and pre-fetching additional data to the cache for future access	712/205
50	US 61700 38 B1	<input checked="" type="checkbox"/>	Trace based instruction caching	711/125
51	US 61675 06 A	<input checked="" type="checkbox"/>	Replacing displacement in control transfer instruction with encoding indicative of target address, including offset and target cache line location	712/213
52	US 61579 98 A	<input checked="" type="checkbox"/>	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
53	US 61579 88 A	<input checked="" type="checkbox"/>	Method and apparatus for high performance branching in pipelined microsystems	711/140
54	US 61346 49 A	<input checked="" type="checkbox"/>	Control transfer indication in predecode which identifies control transfer instruction and an alternate feature of an instruction	712/204
55	US 61227 29 A	<input checked="" type="checkbox"/>	Prefetch buffer which stores a pointer indicating an initial predecode position	712/244
56	US 61192 22 A	<input checked="" type="checkbox"/>	Combined branch prediction and cache prefetch in a microprocessor	712/238
57	US 61192 20 A	<input checked="" type="checkbox"/>	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235
58	US 61087 75 A	<input checked="" type="checkbox"/>	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
59	US 60981 67 A	<input checked="" type="checkbox"/>	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
60	US 60761 44 A	<input checked="" type="checkbox"/>	Method and apparatus for identifying potential entry points into trace segments	711/125
61	US 60732 13 A	<input checked="" type="checkbox"/>	Method and apparatus for caching trace segments with multiple entry points	711/125
62	US 60731 59 A	<input checked="" type="checkbox"/>	Thread properties attribute vector based thread selection in multithreading processor	718/103

	Document ID	U	Title	Current OR
63	US 60617 86 A	<input checked="" type="checkbox"/>	Processor configured to select a next fetch address by partially decoding a byte of a control transfer instruction	712/237
64	US 60386 59 A	<input checked="" type="checkbox"/>	Method for using read-only memory to generate controls for microprocessor	712/226
65	US 60353 87 A	<input checked="" type="checkbox"/>	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
66	US 60322 51 A	<input checked="" type="checkbox"/>	Computer system including a microprocessor having a reorder buffer employing last in buffer and last in line indications	712/216
67	US 60214 89 A	<input checked="" type="checkbox"/>	Apparatus and method for sharing a branch prediction unit in a microprocessor implementing a two instruction set architecture	712/239
68	US 60187 86 A	<input checked="" type="checkbox"/>	Trace based instruction caching	711/4
69	US 60031 42 A	<input checked="" type="checkbox"/>	Test facilitating circuit of microprocessor	714/30
70	US 59481 00 A	<input checked="" type="checkbox"/>	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
71	US 59448 17 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/240
72	US 59352 41 A	<input checked="" type="checkbox"/>	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
73	US 59220 68 A	<input checked="" type="checkbox"/>	Information processing system and information processing method for executing instructions in parallel	712/215
74	US 59180 45 A	<input checked="" type="checkbox"/>	Data processor and data processing system	712/237
75	US 59180 44 A	<input checked="" type="checkbox"/>	Apparatus and method for instruction fetching using a multi-port instruction cache directory	712/235
76	US 59130 49 A	<input checked="" type="checkbox"/>	Multi-stream complex instruction set microprocessor	712/215
77	US 59130 48 A	<input checked="" type="checkbox"/>	Dispatching instructions in a processor supporting out-of-order execution	712/215
78	US 59037 51 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a branch target buffer in CISC processor	712/238
79	US 58899 86 A	<input checked="" type="checkbox"/>	Instruction fetch unit including instruction buffer and secondary or branch target buffer that transfers prefetched instructions to the instruction buffer	712/237
80	US 58871 61 A	<input checked="" type="checkbox"/>	Issuing instructions in a processor supporting out-of-order execution	712/244
81	US 58871 52 A	<input checked="" type="checkbox"/>	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
82	US 58812 60 A	<input checked="" type="checkbox"/>	Method and apparatus for sequencing and decoding variable length instructions with an instruction boundary marker within each instruction	712/210
83	US 58676 98 A	<input checked="" type="checkbox"/>	Apparatus and method for accessing a branch target buffer	712/238
84	US 58646 97 A	<input checked="" type="checkbox"/>	Microprocessor using combined actual and speculative branch history prediction	712/240
85	US 58482 69 A	<input checked="" type="checkbox"/>	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239

	Document ID	U	Title	Current OR
86	US 58450 99 A	<input checked="" type="checkbox"/>	Length detecting unit for parallel processing of variable sequential instructions	712/204
87	US 58357 05 A	<input checked="" type="checkbox"/>	Method and system for performance per-thread monitoring in a multithreaded processor	714/47
88	US 58225 74 A	<input checked="" type="checkbox"/>	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
89	US 58093 20 A	<input checked="" type="checkbox"/>	High-performance multi-processor having floating point unit	712/34
90	US 58092 94 A	<input checked="" type="checkbox"/>	Parallel processing unit which processes branch instructions without decreased performance when a branch is taken	712/233
91	US 58054 75 A	<input checked="" type="checkbox"/>	Load-store unit and method of loading and storing single-precision floating-point registers in a double-precision architecture	708/204
92	US 57969 98 A	<input checked="" type="checkbox"/>	Apparatus and method for performing branch target address calculation and branch prediciton in parallel in an information handling system	712/239
93	US 57940 27 A	<input checked="" type="checkbox"/>	Method and apparatus for managing the execution of instructons with proximate successive branches in a cache-based data processing system	712/238
94	US 57846 04 A	<input checked="" type="checkbox"/>	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
95	US 57685 55 A	<input checked="" type="checkbox"/>	Reorder buffer employing last in buffer and last in line bits	712/216
96	US 57649 40 A	<input checked="" type="checkbox"/>	Processor and method for executing a branch instruction and an associated target instruction utilizing a single instruction fetch	712/206
97	US 57520 14 A	<input checked="" type="checkbox"/>	Automatic selection of branch prediction methodology for subsequent branch instruction based on outcome of previous branch prediction	712/240
98	US 57489 76 A	<input checked="" type="checkbox"/>	Mechanism for maintaining data coherency in a branch history instruction cache	712/240
99	US 57320 05 A	<input checked="" type="checkbox"/>	Single-precision, floating-point register array for floating-point units performing double-precision operations by emulation	708/495
100	US 57154 40 A	<input checked="" type="checkbox"/>	Branch instruction executing device for tracing branch instruments based on instruction type	712/233
101	US 57154 20 A	<input checked="" type="checkbox"/>	Method and system for efficient memory management in a data processing system utilizing a dual mode translation lookaside buffer	711/206
102	US 57064 92 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/238
103	US 56995 38 A	<input checked="" type="checkbox"/>	Efficient firm consistency support mechanisms in an out-of-order execution superscaler multiprocessor	712/23
104	US 56713 82 A	<input checked="" type="checkbox"/>	Information processing system and information processing method for executing instructions in parallel	712/215
105	US 56689 85 A	<input checked="" type="checkbox"/>	Decoder having a split queue system for processing intstructions in a first queue separate from their associated data processed in a second queue	712/245
106	US 56447 44 A	<input checked="" type="checkbox"/>	Superscaler instruction pipeline having boundary identification logic for variable length instructions	712/207
107	US 56425 00 A	<input checked="" type="checkbox"/>	Method and apparatus for controlling instruction in pipeline processor	712/233
108	US 56405 26 A	<input checked="" type="checkbox"/>	Superscaler instruction pipeline having boundary indentification logic for variable length instructions	712/207

	Document ID	U	Title	Current OR
109	US 56341 36 A	<input checked="" type="checkbox"/>	Data processor and method of controlling the same	712/237
110	US 56340 47 A	<input checked="" type="checkbox"/>	Method for executing branch instructions by processing loop end conditions in a second processor	712/241
111	US 56257 87 A	<input checked="" type="checkbox"/>	Superscalar instruction pipeline using alignment logic responsive to boundary identification logic for aligning and appending variable length instructions to instructions stored in cache	712/204
112	US 56257 85 A	<input checked="" type="checkbox"/>	Information processing apparatus having dual buffers for transmitting debug data to an external debug unit	712/227
113	US 56236 15 A	<input checked="" type="checkbox"/>	Circuit and method for reducing prefetch cycles on microprocessors	712/238
114	US 55748 71 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/200
115	US 55111 72 A	<input checked="" type="checkbox"/>	Speculative execution processor	712/235
116	US 55091 30 A	<input checked="" type="checkbox"/>	Method and apparatus for grouping multiple instructions, issuing grouped instructions simultaneously, and executing grouped instructions in a pipelined processor	712/215
117	US 54887 30 A	<input checked="" type="checkbox"/>	Register conflict scoreboard in pipelined computer using pipelined reference counts	712/41
118	US 54816 89 A	<input checked="" type="checkbox"/>	Conversion of internal processor register commands to I/O space addresses	711/202
119	US 54715 91 A	<input checked="" type="checkbox"/>	Combined write-operand queue and read-after-write dependency scoreboard	712/217
120	US 54540 87 A	<input checked="" type="checkbox"/>	Branching system for return from subroutine using target address in return buffer accessed based on branch type information in BHT	712/240
121	US 54505 55 A	<input checked="" type="checkbox"/>	Register logging in pipelined computer using register log queue of register content changes and base queue of register log queue pointers for respective instructions	712/228
122	US 54427 56 A	<input checked="" type="checkbox"/>	Branch prediction and resolution apparatus for a superscalar computer processor	712/238
123	US 54189 17 A	<input checked="" type="checkbox"/>	Method and apparatus for controlling conditional branch instructions for a pipeline type data processing apparatus	712/234
124	US 54148 22 A	<input checked="" type="checkbox"/>	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240
125	US 53945 29 A	<input checked="" type="checkbox"/>	Branch prediction unit for high-performance processor	712/240
126	US 53865 19 A	<input checked="" type="checkbox"/>	Information processing apparatus incorporating buffer storing a plurality of branch target instructions for branch instructions and interrupt requests	712/238
127	US 53815 32 A	<input checked="" type="checkbox"/>	Microprocessor having branch aligner between branch buffer and instruction decoder unit for enhancing initiation of data processing after execution of conditional branch instruction	712/237
128	US 53677 03 A	<input checked="" type="checkbox"/>	Method and system for enhanced branch history prediction accuracy in a superscalar processor system	712/23
129	US 53332 96 A	<input checked="" type="checkbox"/>	Combined queue for invalidates and return data in multiprocessor system	711/171
130	US 53177 20 A	<input checked="" type="checkbox"/>	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143

	Document ID	U	Title	Current OR
131	US 52874 67 A	<input checked="" type="checkbox"/>	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
132	US 52838 73 A	<input checked="" type="checkbox"/>	Next line prediction apparatus for a pipelined computed system	712/207
133	US 52652 13 A	<input checked="" type="checkbox"/>	Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction	712/240
134	US 51971 36 A	<input checked="" type="checkbox"/>	Processing system for branch instruction	712/238
135	US 51558 43 A	<input checked="" type="checkbox"/>	Error transition mode for multi-processor system	714/5
136	US 51519 80 A	<input checked="" type="checkbox"/>	Buffer control circuit for data processor	712/237
137	US 51270 91 A	<input checked="" type="checkbox"/>	System for reducing delay in instruction execution by executing branch instructions in separate processor while dispatching subsequent instructions to primary processor	712/238
138	US 50994 19 A	<input checked="" type="checkbox"/>	Pipeline microcomputer having branch instruction detector and bus controller for producing and carrying branch destination address prior to instruction execution	712/233
139	US 50500 76 A	<input checked="" type="checkbox"/>	Prefetching queue control system	712/219
140	US 49929 32 A	<input checked="" type="checkbox"/>	Data processing device with data buffer control	712/237
141	US 49910 80 A	<input checked="" type="checkbox"/>	Pipeline processing apparatus for executing instructions in three streams, including branch stream pre-execution processor for pre-executing conditional branch instructions	712/206
142	US 49531 21 A	<input checked="" type="checkbox"/>	Circuitry for and method of controlling an instruction buffer in a data-processing system	712/241
143	US 49439 08 A	<input checked="" type="checkbox"/>	Multiple branch analyzer for prefetching cache lines	712/240
144	US 49425 25 A	<input checked="" type="checkbox"/>	Data processor for concurrent executing of instructions by plural execution units	712/217
145	US 48274 02 A	<input checked="" type="checkbox"/>	Branch advanced control apparatus for advanced control of a branch instruction in a data processing system	712/234
146	US 47424 51 A	<input checked="" type="checkbox"/>	Instruction prefetch system for conditional branch instruction for central processor unit	712/235
147	US 47259 47 A	<input checked="" type="checkbox"/>	Data processor with a branch target instruction storage	712/238
148	US 46791 41 A	<input checked="" type="checkbox"/>	Pageable branch history table	712/240
149	US 46046 91 A	<input checked="" type="checkbox"/>	Data processing system having branch instruction prefetching performance	712/207
150	US 43375 10 A	<input checked="" type="checkbox"/>	Read control system for a control storage device	712/211
151	US 42009 27 A	<input checked="" type="checkbox"/>	Multi-instruction stream branch processing mechanism	712/235
152	US 40015 68 A	<input checked="" type="checkbox"/>	Monetary receipt and payment managing apparatus	705/43
153	US 37711 38 A	<input checked="" type="checkbox"/>	APPARATUS AND METHOD FOR SERIALIZING INSTRUCTIONS FROM TWO INDEPENDENT INSTRUCTION STREAMS	712/205

	Docum ent ID	U	Title	Current OR
154	US 36147 47 A	<input type="checkbox"/>	INSTRUCTION BUFFER SYSTEM	711/125

	L #	Hits	Search Text	DBs
1	L1	14876	(instruction prefetch\$3 fetch\$3) near5 (queue buffer)	USPAT; US-PGPUB
2	L2	2862	1 near20 cache	USPAT; US-PGPUB
3	L3	1601	1 near50 branch	USPAT; US-PGPUB
4	L4	2224	1 near20 (select\$3 multiplex\$3)	USPAT; US-PGPUB
5	L8	813	1 near20 target	USPAT; US-PGPUB
6	L12	303	3 near99 8 and 2	USPAT; US-PGPUB
7	L13	242	12 not 7	USPAT; US-PGPUB
8	L7	154	3 near99 4	USPAT; US-PGPUB
9	L14	5468	(instruction prefetch\$3 fetch\$3) near5 (queue buffer)	EPO; JPO; DERWENT; IBM_TDB
10	L15	362	14 near20 cache	EPO; JPO; DERWENT; IBM_TDB
11	L16	377	14 near20 branch	EPO; JPO; DERWENT; IBM_TDB
12	L17	163	14 near20 target	EPO; JPO; DERWENT; IBM_TDB
13	L18	474	14 near20 (select\$3 multiplex\$3)	EPO; JPO; DERWENT; IBM_TDB
14	L22	88	15 and (16 17 18)	EPO; JPO; DERWENT; IBM_TDB
15	L23	67	15 near20 (line block)	EPO; JPO; DERWENT; IBM_TDB
16	L24	11	23 and branch	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 20022 29778 A	<input type="checkbox"/>	PC RELATIVE BRANCHING METHOD WITH HIGH-SPEED DISPLACEMENT	
2	JP 20021 08703 A	<input checked="" type="checkbox"/>	CACHE CONTROLLER AND PROCESSOR	
3	JP 20003 57090 A	<input checked="" type="checkbox"/>	MICROCOMPUTER AND CACHE CONTROL METHOD	
4	JP 20002 15053 A	<input checked="" type="checkbox"/>	CONVERTING METHOD FOR INSTRUCTION STREAM	
5	JP 20002 15048 A	<input checked="" type="checkbox"/>	CONVERTING METHOD FOR INSTRUCTION STREAM	
6	JP 20001 32391 A	<input checked="" type="checkbox"/>	BRANCH PREDICTION MECHANISM	
7	JP 11316 681 A	<input checked="" type="checkbox"/>	LOADING METHOD TO INSTRUCTION BUFFER AND DEVICE AND PROCESSOR THEREFOR	
8	JP 11272 467 A	<input checked="" type="checkbox"/>	METHOD FOR OPERATING SUPERSCALAR PROCESSOR AND CIRCUIT DEVICE	
9	JP 11073 402 A	<input checked="" type="checkbox"/>	BUS BRIDGE CIRCUIT	
10	JP 10214 188 A	<input checked="" type="checkbox"/>	METHOD FOR SUPPLYING INSTRUCTION OF PROCESSOR, AND DEVICE THEREFOR	
11	JP 09091 136 A	<input checked="" type="checkbox"/>	SIGNAL PROCESSOR	
12	JP 09034 786 A	<input checked="" type="checkbox"/>	INSTRUCTION SUPPLYING DEVICE	
13	JP 08190 482 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR SCANNING INSTRUCTION QUEUE	
14	JP 08077 000 A	<input checked="" type="checkbox"/>	CIRCUIT AND METHOD TO REDUCE POWER CONSUMPTION OF SUPER SCALAR PROCESSOR	
15	JP 08069 411 A	<input checked="" type="checkbox"/>	SEMICONDUCTOR DEVICE	
16	JP 08044 563 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
17	JP 08016 468 A	<input checked="" type="checkbox"/>	DATA PREFETCH CONTROL CIRCUIT	
18	JP 08006 853 A	<input checked="" type="checkbox"/>	STORAGE CONTROL METHOD	
19	JP 07210 383 A	<input checked="" type="checkbox"/>	MECHANISM AND METHOD FOR PREDICTING BRANCHING INSTRUCTION	
20	JP 07182 163 A	<input checked="" type="checkbox"/>	SUPER-SCALAR INSTRUCTION DECODING/ISSUING DEVICE	
21	JP 07105 002 A	<input checked="" type="checkbox"/>	COMPUTER SYSTEM	

	Document ID	U	Title	Current OR
22	JP 07073 104 A	<input checked="" type="checkbox"/>	SYSTEM AND METHOD FOR MANAGING EXECUTION OF INSTRUCTION INCLUDING PROXIMATED BRANCHING INSTRUCTION	
23	JP 06110 683 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR EXTENDED BRANCH TARGET OF MICROPROCESSOR	
24	JP 05158 689 A	<input checked="" type="checkbox"/>	BRANCHING PREDICTION DEVICE	
25	JP 04227 542 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
26	JP 04188 245 A	<input checked="" type="checkbox"/>	CACHE MEMORY CONTROLLER	
27	JP 04148 428 A	<input checked="" type="checkbox"/>	MICRO PROCESSOR INTEGRATED CIRCUIT	
28	JP 02239 330 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
29	JP 01088 844 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
30	JP 63163 532 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
31	JP 59079 482 A	<input checked="" type="checkbox"/>	CACHE MEMORY CONTROL SYSTEM	
32	EP 69765 0 A2	<input checked="" type="checkbox"/>	Apparatus and method for instruction queue scanning	
33	EP 64908 6 A1	<input checked="" type="checkbox"/>	Microprocessor with speculative execution.	
34	WO 93173 84 A1	<input checked="" type="checkbox"/>	CPU HAVING PIPELINED INSTRUCTION UNIT AND EFFECTIVE ADDRESS CALCULATION UNIT WITH RETAINED VIRTUAL ADDRESS CAPABILITY	
35	EP 52218 6 A1	<input checked="" type="checkbox"/>	Demultiplexer.	
36	EP 47759 8 A2	<input checked="" type="checkbox"/>	Instruction unit for a processor featuring 'n' processing elements.	
37	EP 47143 4 A2	<input checked="" type="checkbox"/>	Methods and apparatus for controlling a multi-segment cache memory.	
38	EP 47073 6 A1	<input checked="" type="checkbox"/>	Cache memory system.	
39	EP 45740 3 A2	<input checked="" type="checkbox"/>	Multilevel instruction cache, method for using said cache, method for compiling instructions for said cache and micro computer system using such a cache.	
40	EP 27118 7 A2	<input checked="" type="checkbox"/>	Split instruction and operand cache management.	
41	US 66474 67 B	<input checked="" type="checkbox"/>	Branch caching and pipeline controlling method for very long instruction word digital signal processor, involves caching contents of variable number of immediately following prefetch buffers	
42	TW 53837 4 A	<input checked="" type="checkbox"/>	Instruction cache device and method using instruction read buffer - for increasing probability of instruction hit to efficiently access the instruction word in cache instruction word memory	
43	US 66041 91 B	<input checked="" type="checkbox"/>	Instruction fetching system for microprocessor, fetches instruction from sum-addressed instruction cache to provide both target and inline paths	

	Document ID	U	Title	Current OR
44	US 20030 10594 6 A	<input checked="" type="checkbox"/>	Microprocessor selects one copy of broadcast state based on identifier set in microinstruction by microcode sequencer, to process microinstruction	
45	US 65534 83 B	<input checked="" type="checkbox"/>	Register allocation unit for processing system, has controller to generate hit signal when new input value matches value stored in value cache	
46	WO 20027 7822 A	<input checked="" type="checkbox"/>	Monitoring run time execution of software code by inserting routine into buffer with data or cache disabling instruction	
47	US 64271 89 B	<input checked="" type="checkbox"/>	Multi-level cache structure for computer processor, issues predetermined number of entries from data or instruction queues in consecutive clock cycles	
48	US 63670 06 B	<input checked="" type="checkbox"/>	Multiprocessor for computer system, selects next prefetch buffer in response to buffer pointer in previous predecoded buffer	
49	JP 20011 66989 A	<input checked="" type="checkbox"/>	Memory system for computer, performs prefetch of address data relating to prefetch start position of target data, from main memory and stores it in prefetch buffer	
50	US 62232 58 B	<input checked="" type="checkbox"/>	Processor for computer system, has detector circuit to recognize cacheable and non-cacheable instruction based on which bus request is output for allocating buffers	
51	US 62090 58 B	<input checked="" type="checkbox"/>	Data transfer between data disk and cache buffer in cache memory system, involves delaying reading process until pre-fetch data area rotates under transducer, if landing position is outside the data segment	
52	US 61856 69 B	<input checked="" type="checkbox"/>	Hardware embedded run-time optimizer, using Instruction Pointer to Trace Memory (IP-to-TM) cache to map branch targets to optimize traces and determines match by parallel examination of cache and Instruction Translation Lookup Buffer (ITLB)	
53	US 61758 97 B	<input checked="" type="checkbox"/>	Data processing system for pipelined computer central processor, sends instruction to pipeline from instruction buffer, if buffer target address matches with transfer instruction target address	
54	JP 20003 57090 A	<input checked="" type="checkbox"/>	Microcomputer has built-in branch estimation mechanism to reduce access time when cache mistake occurs and precoder to judge branch instruction to be executed	
55	US 61548 33 A	<input checked="" type="checkbox"/>	Branch target buffer hardware conflict handling method in electronic system, involves invalidating instruction pointer associated with branch target buffer cache read that is suppressed due to write allocation	
56	US 60731 59 A	<input checked="" type="checkbox"/>	Multithreading processor selects attributes of threads by locating instruction in proximity with head of instruction queue	
57	US 60121 34 A	<input checked="" type="checkbox"/>	Instruction prefetching apparatus between caches of high speed processor	
58	CN 12260 24 A	<input checked="" type="checkbox"/>	Instruction buffer loading method for superscalar processor, involves assigning fetch address to specific slot of instruction buffer, in which first instruction from cache is stored	
59	EP 93653 9 A	<input checked="" type="checkbox"/>	Process of fetching commands for programmed controlled unit, microprocessor, micro-controller - selectively branches to specific locations in instruction queue when writing instruction data to queue and/or reading instruction data from queue	
60	US 58420 08 A	<input checked="" type="checkbox"/>	Branch target buffer circuit for microprocessor - has branch prediction circuit that indexes all ordered branch target buffer banks of buffer cache, using instruction pointer	
61	US 58227 90 A	<input checked="" type="checkbox"/>	Voting data prefetch system - includes voter coupled to prefetch buffer and selects prefetch address from one of two prefetch predictors based on prediction efficacies, to retrieve data from buffer	

	Document ID	U	Title	Current OR
62	US 58025 94 A	<input checked="" type="checkbox"/>	Instruction translation look-aside buffer for cache of microprocessor - precharges each of hit line during first phase of clock cycle and matches and selects physical address in second phase of cycle	
63	US 57969 98 A	<input checked="" type="checkbox"/>	Instructions fetching apparatus for information handling system - has branch address calculator to which branch queue is coupled for receiving target addresses and addresses of set of fetched instructions	
64	JP 10198 561 A	<input checked="" type="checkbox"/>	Microprocessor using multi-level memory system - has load target buffer containing second entries, which include value which makes second corresponding data fetch instructions correspond to second entry, prevented from producing pre-fetch demand	
65	US 57548 11 A	<input checked="" type="checkbox"/>	Instruction dispatch queue - includes circular dispatch queue with dispatch sequence logic coupled to bottom of dispatch queue pointer for controlling multiplexers so queue outputs instruction from queue to execution unit	
66	US 57348 81 A	<input checked="" type="checkbox"/>	Short Change-Of-Flow detection scheme processor for detecting COF instruction and target instruction are in pre-fetch buffer - has Branch Target Cache which outputs target data in accessed COF entry to pre-fetch unit, and pre-fetch unit which suppresses issue of corresp pre-fetch address if pre-fetch buffer field is valid	
67	EP 92739 4 B	<input checked="" type="checkbox"/>	Branch prediction for a microprocessor instruction cache - has a branch target buffer which shares locations among sets of an instruction cache to store branch information for multiple branch instructions, when a cache line of a set stores more than one branch instruction	
68	JP 09146 835 A	<input checked="" type="checkbox"/>	Data processing system is microprocessor - includes control circuit connected to filter circuit, which controls fetch and prefetch state of buffer circuit from first and second cache memory selectively	
69	JP 09091 136 A	<input checked="" type="checkbox"/>	Signal processing appts for command loop processing - has buffer which is used to store and output instruction to be executed in command loop till end of loop when command cache takes over	
70	JP 08320 788 A	<input checked="" type="checkbox"/>	Pipeline processor for microcomputers - incorporates branch point buffer to monitor and fetch the branched address instruction from cache memory	
71	JP 08286 914 A	<input checked="" type="checkbox"/>	Memory control device for information processing appts - has control unit which determines address of pre memory block which performs next fetch, based on output of decoding unit	
72	US 55532 54 A	<input checked="" type="checkbox"/>	First-in-first-out queue for managing instruction sequence execution - has fields provided in queue element structure for referencing correct instruction cache line but also for specifying cache line sub-sequences and location of branch instructions	
73	EP 71875 8 A	<input checked="" type="checkbox"/>	Cache control unit - includes boundary identification logic to determine nature of byte and anticipation buffer loaded with sequentially anticipated prefetched instructions	
74	JP 08077 000 A	<input checked="" type="checkbox"/>	Computer memory system super scalar microprocessor - has pre-prohibition circuit that controls execution circuit so that pre-buffer corresp. to pre-prohibition signal from cache command is forbidden	
75	US 55155 21 A	<input checked="" type="checkbox"/>	Microprocessor access control unit with fetch address queue - has circuit postponing pending fetch requests from CPU to allow high-priority requests with state machine to provide control signal to address selector	
76	GB 22855 26 A	<input checked="" type="checkbox"/>	Branch instruction prediction mechanism for pipelined microprocessors - addresses information stored by last byte of each branch instruction and sends instruction pointer to branch target buffer circuit when computer fetches block of instructions	
77	US 53353 30 A	<input checked="" type="checkbox"/>	Pipeline information processing appts. with reduced cycle time - adjusts program counter to enable use of otherwise idle buffer storage, so that instructions requiring multiple cycles can be processed in one cycle	
78	US 54993 55 A	<input checked="" type="checkbox"/>	Fast memory access system - has cache memory containing selected data obtained from main memory and buffer storing data that is prefetched before next read request	

	Document ID	U	Title	Current OR
79	EP 62818 4 B	<input checked="" type="checkbox"/>	Digital data processor instruction pre-fetch unit - has branch history table indicates occurrence of branch instruction having target address that was previously taken	
80	EP 52218 6 A	<input checked="" type="checkbox"/>	Multiplexer for cache memories or instruction buffers - selects several adjacent bits, such as four out of sixteen, bytes, half words or words from one register and places them in same order in second register	
81	US 51685 60 A	<input checked="" type="checkbox"/>	Microprocessor system with split operand and instructions cache tag stores - has system tag store with different validity bit for same data line	
82	EP 47143 4 A	<input checked="" type="checkbox"/>	Multi segment cache memory controller - has cache memory segmented to operate at selected working segmentation level	
83	US 52300 68 A	<input checked="" type="checkbox"/>	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	
84	US 49263 23 A	<input checked="" type="checkbox"/>	Streamlined instruction processor for pipelined data - shares address bus between instruction and data accesses with bus being released before transfer is connected	
85	EP 35195 5 A	<input checked="" type="checkbox"/>	Multiprocessor system with cross-interrogated store-in-cache control - uses fetch buffer selectively coupled between memory and requesting processor	
86	EP 34865 2 A	<input checked="" type="checkbox"/>	Checkpoint retry system for processors with cache - has cache pages saved in store buffers following checkpoint	
87	US 48477 53 A	<input checked="" type="checkbox"/>	Pipelined processing instructions computer - compares predicted target address in cache with real target upon branch instruction execution	
88	AU 87798 40 A	<input type="checkbox"/>	Data transfer management system for multiple CPU architecture - implements split instruction and operand cache line-pair state control when program instructions and data are mixed in application program	

	Document ID	U	Title	Current OR
1	JP 20001 32391 A	<input type="checkbox"/>	BRANCH PREDICTION MECHANISM	
2	JP 63163 532 A	<input checked="" type="checkbox"/>	MICROPROCESSOR	
3	EP 71875 8 A2	<input checked="" type="checkbox"/>	Mechanism to identify instruction word boundaries in cache	
4	US 61758 97 B	<input checked="" type="checkbox"/>	Data processing system for pipelined computer central processor, sends instruction to pipeline from instruction buffer, if buffer target address matches with transfer instruction target address	
5	US 57348 81 A	<input checked="" type="checkbox"/>	Short Change-Of-Flow detection scheme processor for detecting COF instruction and target instruction are in pre-fetch buffer - has Branch Target Cache which outputs target data in accessed COF entry to pre-fetch unit, and pre-fetch unit which suppresses issue of corresp pre-fetch address if pre-fetch buffer field is valid	
6	EP 92739 4 B	<input checked="" type="checkbox"/>	Branch prediction for a microprocessor instruction cache - has a branch target buffer which shares locations among sets of an instruction cache to store branch information for multiple branch instructions, when a cache line of a set stores more than one branch instruction	
7	US 55532 54 A	<input checked="" type="checkbox"/>	First-in-first-out queue for managing instruction sequence execution - has fields provided in queue element structure for referencing correct instruction cache line but also for specifying cache line sub-sequences and location of branch instructions	
8	EP 71875 8 A	<input checked="" type="checkbox"/>	Cache control unit - includes boundary identification logic to determine nature of byte and anticipation buffer loaded with sequentially anticipated prefetched instructions	
9	JP 08077 000 A	<input checked="" type="checkbox"/>	Computer memory system super scalar microprocessor - has pre-prohibition circuit that controls execution circuit so that pre-buffer corresp. to pre-prohibition signal from cache command is forbidden	
10	RD 34202 4 A	<input checked="" type="checkbox"/>	Instruction cache accessing method during reload sequence - using cache reload buffer equal to line size of instruction cache to access instruction cache during reload allowing processor to immediately access cache	
11	US 52300 68 A	<input type="checkbox"/>	Integrated instruction-queue and branch-target cache memory - has up to three active instruction queues each associated with sequential instruction stream started by control transfer instruction	

	Document ID	U	Title	Current OR
1	US 20030 23362 5 A1	<input type="checkbox"/>	Method for allocating spare cells in auto-place-route blocks	716/8
2	US 20030 08427 3 A1	<input checked="" type="checkbox"/>	Processor and method of testing a processor for hardware faults utilizing a pipeline interlocking test instruction	712/227
3	US 20030 03350 5 A1	<input checked="" type="checkbox"/>	Apparatus for processing instructions in a computing system	712/215
4	US 20030 00526 2 A1	<input checked="" type="checkbox"/>	Mechanism for providing high instruction fetch bandwidth in a multi-threaded processor	712/207
5	US 20020 19446 4 A1	<input checked="" type="checkbox"/>	Speculative branch target address cache with selective override by secondary predictor based on branch instruction type	712/239
6	US 20020 19446 3 A1	<input checked="" type="checkbox"/>	Speculative hybrid branch direction predictor	712/239
7	US 20020 19446 2 A1	<input checked="" type="checkbox"/>	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
8	US 20020 19446 1 A1	<input checked="" type="checkbox"/>	Speculative branch target address cache	712/238
9	US 20020 19446 0 A1	<input checked="" type="checkbox"/>	Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches	712/238
10	US 20020 18883 4 A1	<input checked="" type="checkbox"/>	Apparatus and method for target address replacement in speculative branch target address cache	712/238
11	US 20020 18883 3 A1	<input checked="" type="checkbox"/>	Dual call/return stack branch prediction system	712/236
12	US 20020 09992 6 A1	<input checked="" type="checkbox"/>	Method and system for prefetching instructions in a superscalar processor	712/207
13	US 20020 09191 6 A1	<input checked="" type="checkbox"/>	Embedded-DRAM-DSP architecture	712/228
14	US 20020 08784 9 A1	<input checked="" type="checkbox"/>	Full multiprocessor speculation mechanism in a symmetric multiprocessor (smp) System	712/235
15	US 20020 08784 5 A1	<input checked="" type="checkbox"/>	Embedded-DRAM-DSP architecture	712/228
16	US 20020 04042 9 A1	<input checked="" type="checkbox"/>	Embedded-DRAM-DSP architecture	712/228
17	US 20010 05413 7 A1	<input checked="" type="checkbox"/>	CIRCUIT ARRANGEMENT AND METHOD WITH IMPROVED BRANCH PREFETCHING FOR SHORT BRANCH INSTRUCTIONS	712/11

	Document ID	U	Title	Current OR
18	US 20010 03744 4 A1	<input checked="" type="checkbox"/>	INSTRUCTION BUFFERING MECHANISM	712/207
19	US 66912 21 B2	<input checked="" type="checkbox"/>	Loading previously dispatched slots in multiple instruction dispatch buffer before dispatching remaining slots for parallel execution	712/215
20	US 66788 20 B1	<input checked="" type="checkbox"/>	Processor and method for separately predicting conditional branches dependent on lock acquisition	712/239
21	US 66585 58 B1	<input checked="" type="checkbox"/>	Branch prediction circuit selector with instruction context related condition type determining	712/239
22	US 66585 34 B1	<input checked="" type="checkbox"/>	Mechanism to reduce instruction cache miss penalties and methods therefor	711/137
23	US 66474 67 B1	<input checked="" type="checkbox"/>	Method and apparatus for high performance branching in pipelined microsystems	711/140
24	US 66041 91 B1	<input checked="" type="checkbox"/>	Method and apparatus for accelerating instruction fetching for a processor	712/207
25	US 65534 82 B1	<input checked="" type="checkbox"/>	Universal dependency vector/queue entry	712/216
26	US 65534 80 B1	<input checked="" type="checkbox"/>	System and method for managing the execution of instruction groups having multiple executable instructions	712/23
27	US 65359 73 B1	<input checked="" type="checkbox"/>	Method and system for speculatively issuing instructions	712/218
28	US 65230 50 B1	<input checked="" type="checkbox"/>	Integer to floating point conversion using one's complement with subsequent correction to eliminate two's complement in critical path	708/204
29	US 64991 23 B1	<input checked="" type="checkbox"/>	Method and apparatus for debugging an integrated circuit	714/724
30	US 64906 06 B1	<input checked="" type="checkbox"/>	Rounding denormalized numbers in a pipelined floating point unit without pipeline stalls	708/497
31	US 64776 40 B1	<input checked="" type="checkbox"/>	Apparatus and method for predicting multiple branches and performing out-of-order branch resolution	712/238
32	US 64426 81 B1	<input checked="" type="checkbox"/>	Pipelined central processor managing the execution of instructions with proximate successive branches in a cache-based data processing system while performing block mode transfer predictions	712/238
33	US 64153 08 B1	<input checked="" type="checkbox"/>	Converting negative floating point numbers to integer notation without two's complement hardware	708/204
34	US 64052 32 B1	<input checked="" type="checkbox"/>	Leading bit prediction with in-parallel correction	708/505
35	US 63935 46 B1	<input checked="" type="checkbox"/>	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
36	US 63816 22 B1	<input checked="" type="checkbox"/>	System and method of expediting bit scan instructions	708/211
37	US 63493 81 B1	<input checked="" type="checkbox"/>	Pipelined instruction dispatch unit in a superscalar processor	712/215
38	US 63321 91 B1	<input checked="" type="checkbox"/>	System for canceling speculatively fetched instructions following a branch mis-prediction in a microprocessor	712/240
39	US 63082 59 B1	<input checked="" type="checkbox"/>	Instruction queue evaluating dependency vector in portions during different clock phases	712/214

	Document ID	U	Title	Current OR
40	US 62667 63 B1	<input checked="" type="checkbox"/>	Physical rename register for efficiently storing floating point, integer, condition code, and multimedia values	712/36
41	US 62667 52 B1	<input checked="" type="checkbox"/>	Reverse TLB for providing branch target address in a microprocessor having a physically-tagged cache	711/200
42	US 62533 16 B1	<input checked="" type="checkbox"/>	Three state branch history using one bit in a branch prediction mechanism	712/239
43	US 62471 24 B1	<input checked="" type="checkbox"/>	Branch prediction entry with target line index calculated using relative position of second operation of two step branch operation in a line of instructions	712/240
44	US 62471 06 B1	<input checked="" type="checkbox"/>	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	711/203
45	US 62370 85 B1	<input checked="" type="checkbox"/>	Processor and method for generating less than (LT), Greater than (GT), and equal to (EQ) condition code bits concurrent with a logical or complex operation	712/223
46	US 62328 72 B1	<input checked="" type="checkbox"/>	Comparator	340/146 .2
47	US 62302 62 B1	<input checked="" type="checkbox"/>	Processor configured to selectively free physical registers upon retirement of instructions	712/244
48	US 62197 73 B1	<input checked="" type="checkbox"/>	System and method of retiring misaligned write operands from a write buffer	711/201
49	US 62126 29 B1	<input checked="" type="checkbox"/>	Method and apparatus for executing string instructions	712/241
50	US 62126 23 B1	<input checked="" type="checkbox"/>	Universal dependency vector/queue entry	712/216
51	US 62126 22 B1	<input checked="" type="checkbox"/>	Mechanism for load block on store address generation	712/216
52	US 62055 60 B1	<input checked="" type="checkbox"/>	Debug system allowing programmable selection of alternate debug mechanisms such as debug handler, SMI, or JTAG	714/34
53	US 61924 65 B1	<input checked="" type="checkbox"/>	Using multiple decoders and a reorder queue to decode instructions out of order	712/212
54	US 61758 97 B1	<input checked="" type="checkbox"/>	Synchronization of branch cache searches and allocation/modification/deletion of branch cache	711/119
55	US 61579 98 A	<input checked="" type="checkbox"/>	Method for performing branch prediction and resolution of two or more branch instructions within two or more branch prediction buffers	712/238
56	US 61579 88 A	<input checked="" type="checkbox"/>	Method and apparatus for high performance branching in pipelined microsystems	711/140
57	US 61417 47 A	<input checked="" type="checkbox"/>	System for store to load forwarding of individual bytes from separate store buffer entries to form a single load word	712/225
58	US 61382 30 A	<input checked="" type="checkbox"/>	Processor with multiple execution pipelines using pipe stage state information to control independent movement of instructions between pipe stages of an execution pipeline	712/216
59	US 61227 27 A	<input checked="" type="checkbox"/>	Symmetrical instructions queue for high clock frequency scheduling	712/214
60	US 61226 56 A	<input checked="" type="checkbox"/>	Processor configured to map logical register numbers to physical register numbers using virtual register numbers	718/100
61	US 61192 23 A	<input checked="" type="checkbox"/>	Map unit having rapid misprediction recovery	712/244
62	US 61192 20 A	<input checked="" type="checkbox"/>	Method of and apparatus for supplying multiple instruction strings whose addresses are discontinued by branch instructions	712/235

	Document ID	U	Title	Current OR
63	US 61087 75 A	<input checked="" type="checkbox"/>	Dynamically loadable pattern history tables in a multi-task microprocessor	712/240
64	US 60790 05 A	<input checked="" type="checkbox"/>	Microprocessor including virtual address branch prediction and current page register to provide page portion of virtual and physical fetch address	711/213
65	US 60790 03 A	<input checked="" type="checkbox"/>	Reverse TLB for providing branch target address in a microprocessor having a physically-tagged cache	711/200
66	US 60761 46 A	<input checked="" type="checkbox"/>	Cache holding register for delayed update of a cache line into an instruction cache	711/125
67	US 60732 31 A	<input checked="" type="checkbox"/>	Pipelined processor with microcontrol of register translation hardware	712/218
68	US 60353 90 A	<input checked="" type="checkbox"/>	Method and apparatus for generating and logically combining less than (LT), greater than (GT), and equal to (EQ) condition code bits concurrently with the execution of an arithmetic or logical operation	712/220
69	US 60353 87 A	<input checked="" type="checkbox"/>	System for packing variable length instructions into fixed length blocks with indications of instruction beginning, ending, and offset within block	712/210
70	US 60165 45 A	<input checked="" type="checkbox"/>	Reduced size storage apparatus for storing cache-line-related data in a high frequency microprocessor	712/238
71	US 59960 71 A	<input checked="" type="checkbox"/>	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
72	US 59833 21 A	<input checked="" type="checkbox"/>	Cache holding register for receiving instruction packets and for providing the instruction packets to a predecode unit and instruction cache	711/125
73	US 59742 60 A	<input checked="" type="checkbox"/>	Data processor to control a sequence of instructions to be executed by rearranging the instruction blocks	712/32
74	US 59639 84 A	<input checked="" type="checkbox"/>	Address translation unit employing programmable page size	711/206
75	US 59580 42 A	<input checked="" type="checkbox"/>	Grouping logic circuit in a pipelined superscalar processor	712/215
76	US 59548 15 A	<input checked="" type="checkbox"/>	Invalidating instructions in fetched instruction blocks upon predicted two-step branch operations with second operation relative target address	712/237
77	US 59481 00 A	<input checked="" type="checkbox"/>	Branch prediction and fetch mechanism for variable length instruction, superscalar pipelined processor	712/238
78	US 59467 05 A	<input checked="" type="checkbox"/>	Avoidance of cache synonyms	711/108
79	US 59448 17 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/240
80	US 59371 78 A	<input checked="" type="checkbox"/>	Register file for registers with multiple addressable sizes using read-modify-write for register file update	712/218
81	US 59352 41 A	<input checked="" type="checkbox"/>	Multiple global pattern history tables for branch prediction in a microprocessor	712/240
82	US 59180 05 A	<input checked="" type="checkbox"/>	Apparatus region-based detection of interference among reordered memory operations in a processor	714/38
83	US 59078 60 A	<input checked="" type="checkbox"/>	System and method of retiring store data from a write buffer	711/117
84	US 59037 51 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a branch target buffer in CISC processor	712/238

	Document ID	U	Title	Current OR
85	US 58570 89 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
86	US 58420 08 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a branch target buffer cache with multiple BTB banks	712/240
87	US 58388 97 A	<input checked="" type="checkbox"/>	Debugging a processor using data output during idle bus cycles	714/30
88	US 58359 67 A	<input checked="" type="checkbox"/>	Adjusting prefetch size based on source of prefetch address	711/213
89	US 58359 51 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache read prioritization protocol for handling multiple hits	711/145
90	US 58359 49 A	<input checked="" type="checkbox"/>	Method of identifying and self-modifying code	711/135
91	US 58058 79 A	<input checked="" type="checkbox"/>	In a pipelined processor, setting a segment access indicator during execution stage using exception handling	712/244
92	US 57940 26 A	<input checked="" type="checkbox"/>	Microprocessor having expedited execution of condition dependent instructions	712/236
93	US 57845 89 A	<input checked="" type="checkbox"/>	Distributed free register tracking for register renaming using an availability tracking register associated with each stage of an execution pipeline	712/217
94	US 57845 86 A	<input checked="" type="checkbox"/>	Addressing method for executing load instructions out of order with respect to store instructions	712/216
95	US 57817 53 A	<input checked="" type="checkbox"/>	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
96	US 57747 10 A	<input checked="" type="checkbox"/>	Cache line branch prediction scheme that shares among sets of a set associative cache	712/238
97	US 57713 65 A	<input checked="" type="checkbox"/>	Condensed microaddress generation in a complex instruction set computer	712/205
98	US 57685 75 A	<input checked="" type="checkbox"/>	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/228
99	US 57649 38 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/200
100	US 57522 74 A	<input checked="" type="checkbox"/>	Address translation unit employing a victim TLB	711/206
101	US 57489 76 A	<input checked="" type="checkbox"/>	Mechanism for maintaining data coherency in a branch history instruction cache	712/240
102	US 57489 32 A	<input checked="" type="checkbox"/>	Cache memory system for dynamically altering single cache memory line as either branch target entry or prefetch instruction queue based upon instruction sequence	715/526
103	US 57427 55 A	<input checked="" type="checkbox"/>	Error-handling circuit and method for memory address alignment double fault	714/53
104	US 57404 16 A	<input checked="" type="checkbox"/>	Branch processing unit with a far target cache accessed by indirection from the target cache	712/238
105	US 57404 15 A	<input checked="" type="checkbox"/>	Instruction supplying apparatus with a branch target buffer having the contents so updated as to enhance branch prediction accuracy	712/238

	Document ID	U	Title	Current OR
106	US 57403 98 A	<input checked="" type="checkbox"/>	Program order sequencing of data in a microprocessor with write buffer	711/117
107	US 57348 81 A	<input checked="" type="checkbox"/>	Detecting short branches in a prefetch buffer using target location information in a branch target cache	712/238
108	US 57322 53 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache storing history for predicted taken branches and history cache storing history for predicted not-taken branches	712/239
109	US 57322 43 A	<input checked="" type="checkbox"/>	Branch processing unit with target cache using low/high banking to support split prefetching	711/137
110	US 57087 88 A	<input checked="" type="checkbox"/>	Method for adjusting fetch program counter in response to the number of instructions fetched and issued	712/214
111	US 57064 92 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/238
112	US 57064 91 A	<input checked="" type="checkbox"/>	Branch processing unit with a return stack including repair using pointers from different pipe stages	712/234
113	US 57014 48 A	<input checked="" type="checkbox"/>	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
114	US 56969 55 A	<input checked="" type="checkbox"/>	Floating point stack and exchange instruction	712/222
115	US 56921 68 A	<input checked="" type="checkbox"/>	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
116	US 56871 10 A	<input checked="" type="checkbox"/>	Array having an update circuit for updating a storage location with a value stored in another storage location	365/154
117	US 56492 25 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/23
118	US 56447 41 A	<input checked="" type="checkbox"/>	Processor with single clock decode architecture employing single microROM	712/200
119	US 56301 49 A	<input checked="" type="checkbox"/>	Pipelined processor with register renaming hardware to accommodate multiple size registers	712/217
120	US 56236 15 A	<input checked="" type="checkbox"/>	Circuit and method for reducing prefetch cycles on microprocessors	712/238
121	US 56236 14 A	<input checked="" type="checkbox"/>	Branch prediction cache with multiple entries for returns having multiple callers	712/240
122	US 56154 02 A	<input checked="" type="checkbox"/>	Unified write buffer having information identifying whether the address belongs to a first write operand or a second write operand having an extra wide latch	712/38
123	US 56110 71 A	<input checked="" type="checkbox"/>	Split replacement cycles for sectored cache lines in a 64-bit microprocessor interfaced to a 32-bit bus architecture	711/133
124	US 56049 09 A	<input checked="" type="checkbox"/>	Apparatus for processing instructions in a computing system	712/208
125	US 55967 40 A	<input checked="" type="checkbox"/>	Interleaved memory conflict resolution with accesses of variable bank widths and partial return of non-conflicting banks	711/157
126	US 55967 35 A	<input checked="" type="checkbox"/>	Circuit and method for addressing segment descriptor tables	712/239
127	US 55967 31 A	<input checked="" type="checkbox"/>	Single clock bus transfers during burst and non-burst cycles	710/305
128	US 55840 09 A	<input checked="" type="checkbox"/>	System and method of retiring store data from a write buffer	711/117

	Document ID	U	Title	Current OR
129	US 55748 71 A	<input checked="" type="checkbox"/>	Method and apparatus for implementing a set-associative branch target buffer	712/200
130	US 55532 55 A	<input checked="" type="checkbox"/>	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
131	US 54715 98 A	<input checked="" type="checkbox"/>	Data dependency detection and handling in a microprocessor with write buffer	711/122
132	US 54540 87 A	<input checked="" type="checkbox"/>	Branching system for return from subroutine using target address in return buffer accessed based on branch type information in BHT	712/240
133	US 54349 85 A	<input checked="" type="checkbox"/>	Simultaneous prediction of multiple branches for superscalar processing	712/240
134	US 53718 64 A	<input checked="" type="checkbox"/>	Apparatus for concurrent multiple instruction decode in variable length instruction set computer	712/206
135	US 53534 26 A	<input checked="" type="checkbox"/>	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
136	US 52838 73 A	<input checked="" type="checkbox"/>	Next line prediction apparatus for a pipelined computed system	712/207
137	US 52300 68 A	<input checked="" type="checkbox"/>	Cache memory system for dynamically altering single cache memory line as either branch target entry or pre-fetch instruction queue based upon instruction sequence	711/137
138	US 52108 31 A	<input checked="" type="checkbox"/>	Methods and apparatus for insulating a branch prediction mechanism from data dependent branch table updates that result from variable test operand locations	712/240
139	US 49910 80 A	<input checked="" type="checkbox"/>	Pipeline processing apparatus for executing instructions in three streams, including branch stream pre-execution processor for pre-executing conditional branch instructions	712/206
140	US 49439 08 A	<input checked="" type="checkbox"/>	Multiple branch analyzer for prefetching cache lines	712/240
141	US 49263 23 A	<input type="checkbox"/>	Streamlined instruction processor	712/238